Remarks

The Examiner has subjected claims 8-31 to four separate restriction requirements wherein the Applicant is required to elect a single disclosed species for prosecution on the merits. In particular, Applicant must elect a single disclosed species in the subject matter defined by claims 17-19, the subject matter defined by claims 20 and 21, the subject matter of claims defined by claims 24 and 25 and the subject matter of claims defined by claims 26 and 27.

Regarding the Restriction Requirement

Applicant respectfully traverses each of the four separate restriction requirements, and in compliance with the requirement of restriction, Applicant hereby elects the subject matter of claim 17 (rigid body), claim 20 (solder ball), claim 24 (parametric testing), and claim 27 (simultaneously). Applicant reserves the right to file a divisional application on the non-elected subject matter.

With respect to the subject matter of claims 17-19, a restriction requirement is improper as a search and examination of the subject matter of claims 17-19 can be made without serious burden. The MPEP states the following the respect to a proper restriction requirement:

> Under the statute an application may properly be required to be restricted to one of two or more claimed inventions

> only if they are able to support separate patents and they are either independent (MPEP §806.04-§806.04(i)) or distinct (MPEP §806.05-§806.05(i)).
>
> **If the search and examination of an entire application can be made without serious burden, the examiner must examine it on the merits, even though it includes claims to independent or distinct inventions.** Emphasis added. MPEP §803.

The Examiner has taken the position that claims 17, 18 and 19 are patentably distinct inventions requiring separate searches and examinations. If claim 17 was written in independent format, it would read as follows:

> A method for producing a wafer-interposer assembly comprising the steps of:
> attaching one or more first electrical contacts to a lower surface of a substrate, the substrate comprising a B-Stage adhesive material that forms **a rigid bond;**
> attaching one or more second electrical contacts to an upper surface of the substrate, the second electrical contacts having greater surface area and greater pitch than the first electrical contacts;
> creating one or more first electrical pathways through the substrate and connecting the first electrical contacts to the second electrical contacts;
> depositing a conductor on one or more third electrical contacts on an upper surface of a semiconductor wafer, the semiconductor wafer including one or more semiconductor dies and the third electrical contacts being associated with the semiconductor dies;
> applying a layer of no-flow underfill to the upper surface of the semiconductor wafer;
> aligning the substrate with the semiconductor wafer so that the deposits of the conductor on the third electrical contacts correspond with the first electrical contacts on the lower surface of the substrate;
> attaching the substrate to the semiconductor wafer.

If claim 18 was written in independent format, it would read as follows:

A method for producing a wafer-interposer assembly comprising the steps of:

attaching one or more first electrical contacts to a lower surface of a substrate, the substrate comprising a B-Stage adhesive material that forms **a semi-rigid bond**;

attaching one or more second electrical contacts to an upper surface of the substrate, the second electrical contacts having greater surface area and greater pitch than the first electrical contacts;

creating one or more first electrical pathways through the substrate and connecting the first electrical contacts to the second electrical contacts;

depositing a conductor on one or more third electrical contacts on an upper surface of a semiconductor wafer, the semiconductor wafer including one or more semiconductor dies and the third electrical contacts being associated with the semiconductor dies;

applying a layer of no-flow underfill to the upper surface of the semiconductor wafer;

aligning the substrate with the semiconductor wafer so that the deposits of the conductor on the third electrical contacts correspond with the first electrical contacts on the lower surface of the substrate;

attaching the substrate to the semiconductor wafer.

Similarly, if claim 19 was written in independent format, it would read as follows:

> A method for producing a wafer-interposer assembly comprising the steps of:
> attaching one or more first electrical contacts to a lower surface of a substrate, the substrate comprising a B-Stage adhesive material that forms **a compliant bond**;
> attaching one or more second electrical contacts to an upper surface of the substrate, the second electrical contacts having greater surface area and greater pitch than the first electrical contacts;
> creating one or more first electrical pathways through the substrate and connecting the first electrical contacts to the second electrical contacts;
> depositing a conductor on one or more third electrical contacts on an upper surface of a semiconductor wafer, the semiconductor wafer including one or more semiconductor dies and the third electrical contacts being associated with the semiconductor dies;
> applying a layer of no-flow underfill to the upper surface of the semiconductor wafer;
> aligning the substrate with the semiconductor wafer so that the deposits of the conductor on the third electrical contacts correspond with the first electrical contacts on the lower surface of the substrate;
> attaching the substrate to the semiconductor wafer.

For the Examiner's convenience, the differences between the claims are bolded. The search and examination of each of these claims may be made without serious burden as a unity of invention exists between the claims with respect to the B-stage adhesive. The B-stage adhesive, whether rigid, semi-rigid or compliant, in each of the claims shares a common utility and structure, i.e., a bonding with the lower substrate. As the B-stage adhesive in each of the claims shares a common utility and structure, unity of invention exists. Accordingly, the search and examination of each of these claims may be made without serious burden. Hence,

Applicant respectfully requests that the outstanding restriction requirement be withdrawn.

With respect to the subject matter of claims 20 and 21, a restriction requirement is improper as a search and examination of the subject matter of claims 20 and 21 can be made without serious burden. Similar to claims 17-19, a unity of invention exists between claims 20 and 21 that enables a search and examination to be conducted on claims 20 and 21 without serious burden. Claims 20 and 21 include limitations directed to a common utility and structure, i.e., the specific composition, solder ball or conductive-polymer adhesive, of a conductor. Accordingly, the search and examination of each of these claims may be made without serious burden. Hence, Applicant respectfully requests that the outstanding restriction requirement be withdrawn.

With respect to the subject matter of claims 24 and 25, a restriction requirement is improper as a search and examination of the subject matter of claims 24 and 25 can be made without serious burden. Similar to claims 17-19, a unity of invention exists between claims 24 and 25 that enables a search and examination to be conducted without serious burden. Claims 24 and 25 include limitations directed to a common utility, i.e., the step of testing semiconductor dies by parametric testing or burn-in testing. Accordingly, the search and examination of each of these claims may

be made without serious burden. Hence, Applicant respectfully requests that the outstanding restriction requirement be withdrawn.

With respect to the subject matter of claims 26 and 27, a restriction requirement is improper as a search and examination of the subject matter of claims 26 and 27 can be made without serious burden. Similar to claims 17-19, a unity of invention exists between claims 26 and 27 that enables a search and examination to be conducted without serious burden. Claims 26 and 27 include limitations directed to a common utility, i.e., the step of testing semiconductor dies sequentially or simultaneously. Accordingly, the search and examination of each of these claims may be made without serious burden. Hence, Applicant respectfully requests that the outstanding restriction requirement be withdrawn.

Fee Statement

Form PTO-2038 is submitted herewith authorizing the Commissioner to charge $205.00 to the indicated account for an Extension for Response within Two Months per 37 C.F.R. §1.17(a)(2). Accordingly, Applicant believes no additional fees are due for the filing of this Response. However, if any additional fees are due, or any overpayments have been made, please charge, or credit, our Deposit Account No. 03-1130.

Conclusion

The Examiner is requested to call the undersigned for any reason that would advance the instant application to issue.

Dated this 19th day of March, 2003.

Respectfully submitted:

Lawrence R. Youst
Reg. No. 38,795
Danamraj & Youst, P.C.
12900 Preston Road
Suite 1200, LB-15
Dallas, Texas 75230
Tel 972.392.2696
Fax 972.720.1139